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Harold C. Moore
Name of person mailing Document or Fee

Signature

December 8, 2003
Date of Signature

Re:	Application of:	Chiesl
	Serial No.:	09/960,441
	Filed:	September 21, 2001
	For:	Arrangement for Measuring Pressure on a Semiconductor Wafer and an Associated Method for Fabricating a Semiconductor Wafer
	Group Art Unit:	2812
	Examiner:	Viktor Simkovic
	Our Docket No.:	1003-0610
	LSI Docket No.:	01-384

TRANSMITTAL OF BRIEF ON APPEAL

Please find for filing in connection with the above patent application the following documents:

1. Original of the Appeal Brief;

2. Three (3) copies of the Appeal Brief; and

3. One (1) return post card.

The Commissioner is hereby authorized to charge the filing fee of an Appeal Brief ($330.00) as required by 37 C.F.R. § 1.17(e) to **Deposit Account No. 12-2252.**

Please charge any fee deficiency, or credit any overpayment, to Deposit Account No. 12-2252 but not to include any payment of issue fees.

Respectfully Submitted,

MAGINOT, MOORE & BECK, LLP

December 8, 2003

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Enclosures

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Re:	Application of:	Newell E. Chiesl
	Serial No.:	09/960,441
	Filed:	September 21, 2001
	Confirmation No.:	5776
	For:	Arrangement for Measuring Pressure on a Semiconductor Wafer and an Associated Method for Fabricating a Semiconductor Wafer
	Group Art Unit:	2812
	Examiner:	Viktor Simkovic
	Our Docket:	1003-0610

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BRIEF ON APPEAL

Sir:

This is an appeal under 37 CFR § 1.191 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the final rejection of claims 17, 19, 20 and 22-28 of the above-identified patent application. These claims were indicated as finally

rejected in an Office Action dated June 25, 2003. Three copies of the brief are filed herewith. Please charge Deposit Account No. 12-2232 to cover the fee required under 37 CFR § 1.17(f).

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There are no appeals or interferences related to this patent application.

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Claims 1-17 and 19-28 are pending in the application.

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(5) SUMMARY OF THE INVENTION

Claim 17 is directed to a method of fabricating a semiconductor wafer, including subjecting the semiconductor wafer to a pressure. The pressure the semiconductor wafer is subjected to is measured with a pressure measurement device supported on the semiconductor wafer. (See, e.g. specification at p.10, lines 15-20). The pressure measurement device includes (i) a capacitor (see, e.g. Fig. 53 and specification at p.12, lines 7-9), (ii) capacitance measurement circuitry electrically coupled to the capacitor (see, e.g. Fig. 53 and specification at p. 11, lines 10-14), and (iii) capacitance to pressure conversion circuitry electrically coupled to the capacitance measurement circuitry (see e.g. *id.*)

Claim 19 further recites that pressure data storage circuitry is supported on the semiconductor wafer, and that this circuitry is electrically coupled to the capacitance to pressure conversion circuitry. (See, e.g. Fig. 53 and specification at p.11, lines 16-20). Claim 20 further recites transmission of pressure information to a receiver using an on-chip transmitter. (See, e.g. Fig. 53 and specification at p.20, lines 8-14).

In other embodiments, the method of the invention includes first forming the capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first

and second metal plates separated by a void. (See, e.g. plates 32, 34 of Fig. 20 and specification at p.14, lines 12-20). In yet other embodiments, a protecting layer is supported on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer. This provides protection of the metal plate of the capacitor from exposure to certain substances. (See, e.g. specification at p.14, line 21 to p.16, line 2.)

(6) ISSUES

Whether claims 17 and 19-20 are unpatentable under 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,444,637 to Smesny et al. (hereinafter "Smesny") in view of U.S. Patent No. 6,378,378 to Fisher (hereinafter "Fisher");

Whether claims 27 and 28 are unpatentable under 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,719,069 to Sparks (hereinafter "Sparks");

Whether 25 and 26 are unpatentable under 35 U.S.C. § 103 as obvious over Smesny in view of Fisher in further view of Sparks.

(7) GROUPING OF CLAIMS

The claims do not all stand or fall together.

Claims 17, 19 and 20 form a first separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 27 forms a second separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 28 forms a third separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 25 forms a fourth separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 26 forms a fifth separately patentable group which is argued independently of the other claims for purposes of this appeal.

(8) ARGUMENT

First Claim Grouping: Claims 17, 19 and 20 Are Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 17

1. Claim 17

Claim 17 includes the following limitations:

> measuring said pressure said semiconductor is subjected to with a pressure measurement device supported on said semiconductor wafer, said pressure measurement device including (i) a capacitor, (ii) capacitance measurement circuitry electrically coupled to said capacitor;

2. Smesny Does Not Teach Measuring Pressure with a Capacitor

As admitted by the Examiner, Smesny does not teach or suggest measuring pressure with the pressure measurement device that includes a capacitor and a capacitance measurement circuit electrically coupled to the capacitor. (See e.g. June 25, 2003 Office Action at p.3). Smesny instead suggests that sensors may be implemented to measure pressure conditions on a semiconductor, wherein the pressure sensors may comprise transducers that include resistive circuits. (See Smesny at col. 9, lines 32-44).

3. <u>No Motivation or Suggestion to Modify Smesny With Fisher</u>

Instead, the Examiner relies on Fisher to provide the teaching that a pressures sensor disposed on the semiconductor of Smesny may be a capacitive MEMs pressure sensor. (See June 25, 2003 Office Action at p.3). However, it is respectfully submitted that there is no legally sufficient motivation or suggestion to combine the use of a capacitive MEMs pressure sensor as taught by Fisher in the device of Smesny.

In particular, the Examiner set forth the following reasoning for combining Smesny and Fisher:

> What Smesny et al. fail to specifically teach is the use of a capacitive pressure sensor. This is taught by Fisher in column 3, lines 21-27, where Fisher specifically mentions "capacitive MEMs pressure sensors". . . . Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a capacitive pressure sensor with the method of Smesny et al., since this type of sensor is well suited to be incorporated onto a substrate, as Fisher suggests.

(June 25, 2003 office action at p.3) (emphasis added).

Applicant submits that Fisher does not teach that a capacitive pressure sensor is "well suited" for use in Smesny. Smesny specifically teaches the use of sensors that are *fabricated* in the silicon wafer. Smesny does not suggest or imply that sensors may be separately fabricated and then attached to the semiconductor using adhesives. Yet Fisher only teaches that capacitive MEMs pressures sensors can be separately formed and then attached by adhesives. There is no motivation or suggestion that capacitive MEMs pressure sensors may be "fabricated upon" the wafer of Smesny, nor that it is advantageous to abandon the teachings of Smesny and instead use separately fabricated sensors and attach them to the wafer using an adhesive.

More specifically, Smesny clearly teaches the use of integrally formed sensors, which is much different than separately assembling sensors onto the substrate. Referring to Smesny:

> Sensors 12 described herein are necessary for detecting various processing conditions, and are *fabricated upon* wafer 10 according to well known semiconductor transducer design.
> . .

. . .

> Sensors 12 may also be used to measure pressure, force or strain placed at select regions across wafer 10. There are may types of pressure transducers capable of measuring the atmospheric pressure exerted upon the wafer. A suitable pressure transducer includes a diaphragm-type transducer, wherein a diaphragm or elastic element senses pressure and produces a corresponding strain or deflection which can then be read by a bridge circuit connected to the diaphragm or cavity behind the diaphragm. *Another suitable pressure transducer may include a piezoresistive material placed within the semiconductor substrate of wafer 10. The piezoresistive material is formed by diffusing doping compounds into the substrate.* The resulting piezoresistive material produces output current proportional to the amount of pressure or strain exerted thereupon.

(Smesny at col. 8, lines 63-66 and col. 9, lines 28-43) (emphasis added).

Thus, Smesny specifically teaches the use of integrally formed sensors that are fabricated on the substrate. There is no suggestion that separately formed sensors (attached by adhesive) will be suitable or desirable for the circuit of Smesny.

By contrast, Fisher clearly teaches that when capacitive sensors are use, they are used as separately fabricated sensors that are attached using adhesives:

> A number of pressure sensors 12 have been attached to a surface 14 of the wafer with epoxy adhesive 16. The sensors could be attached to the wafer using other adhesives, such as silicone or urethane adhesives. The sensors could be a variety of sensors, such as capacitive MEMS pressure sensors . . . .
>
> . . .
>
> The sensors are packaged pressure sensors, such as the Model 7000-1 sold by ADVANCED CUSTOME SENSORS, INC., the Model EPI-41 sold by ENRAN®, SENSEON™ pressure sensors sold by MOTOROLA, or similar sensors.

(Fisher at col. 3, lines 21-41)

Thus, to the extent Fisher teaches the use of a capacitive sensor, it teaches a *separately-formed* capacitive sensor, which is *not* suitable for use in Smesny. While separately formed sensors may be useful in Fisher, where none of the conversion or data circuitry is located on the chip, such separately formed sensors would be less useful in Smesny, where more circuitry and a greater number of sensors are employed on chip.

To this end, Fisher itself suggests that separately formed sensors are not suitable for use in wafers that incorporate additional conversion and processing circuitry for the pressure measurements. In particular, Fisher discloses one embodiment that does in fact employ integrally formed sensors, although the integrally formed sensors are not *capacitive* pressure sensors. (Fisher at col. 4, line 40 to col. 5, line 26). In any event, Fisher teaches that if integrated (i.e. non-capacitive) sensors, are used, then other circuits may be included on the wafer, including circuits that balance, amplify or buffer the sensor signals. (*Id.* at col. 4, lines 61-65). The clear implication is that the use of *separately* fabricated sensors does *not* lend itself to the inclusion of other supporting circuitry.

Because Fisher only teaches the use of capacitive pressure sensors that are separately fabricated, the resulting teaching of Fisher is that capacitive pressure sensors are not suitable for wafers that include other circuitry that assists in obtaining or processing the measured pressure information. Because Smesny teaches a circuit that employs such other circuitry, including a signal conditioning circuit and a processor, Fisher would only suggest, if anything, the use of integrally-formed, non-capacitive sensors, and not separately fabricated capacitive sensors.

For the above reasons, it is respectfully submitted that the Examiner has failed to make out a prima facie case of obviousness. Specifically, there is no legally sufficient motivation or suggestion in the prior art to employ the capacitive MEMS pressure sensors into the circuit disclosed in Smesny. As a consequence, the rejection of claim 17 should be reversed.

Discussion re: Patentability of Claim 19 and 20

Claims 19 and 20 both depend from and incorporate all of the limitations of claim 17. Accordingly, for at least the same reasons as those set forth above in connection with claim 17, it is respectfully submitted that claims 19 and 20 are patentable over the prior art.

Second Claim Grouping: Claims 27 is not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 27

1. Claim 27

Claim 27 includes the following limitations:

(a) forming a capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor wafer, the first and second metal plates separated by a void;

(b) subjecting said semiconductor wafer to a pressure; and

(c) measuring said pressure said semiconductor wafer is subjected to using the capacitor

2. Sparks Does Not Teach Use of a Capacitor to Measure Pressure

Sparks does not teach or suggest the use of a capacitor to measure pressure, as required by step (c) of claim 27. Nevertheless, in the June 25, 2003 office action, the Examiner provided the following reasoning for the obviousness rejection:

> Sparks teaches a method of forming a semiconductor wafer by fabricating first and second metal plates on the wafer separated by a void (Fig. 4). Sparks does not specifically include the steps of subjecting the wafer to pressure and measuring said pressure using the capacitor, but this is in fact the method of using the pressure sensor taught by Sparks. It would have been obvious to one or ordinary skill in the art at the time of the invention to use the pressure sensor in this way.

(June 25, 2004 office action at pp.3-4)

Applicants disagree that the device illustrated in Fig. 4 of Sparks represents a pressure sensor. The illustrated device indeed has first and second metal plates, but it is not a pressure sensor. The device of Fig. 4 of Sparks is an accelerometer. (Sparks at col. 3, lines 66-67). As a consequence, the Examiner's reasoning that it would have been obvious to "use the pressure sensor in this way" is based on an incorrect premise.

Nevertheless, Sparks does teach a pressure sensor. However, that pressure sensor is piezoresistive, not capacitive. (Sparks at col. 3, lines 53-55). Thus, while it may have been obvious to measure pressure using the *piezoresistive* pressure sensor of Sparks (Fig. 1), there is no teaching to measure pressure using the capacitive accelerometer of Fig. 4. The use of the piezoresistive pressure sensor of Sparks to measure pressure does not arrive at the invention of claim 27.

A pressure sensor and an accelerometer are not the same device. To this end, Sparks clearly distinguishes between pressure sensors and accelerometers, highlighting that those devices are *not* one in the same. (E.g. *id.* at col. 3, lines 53-67 and col. 4, lines 8-17).

Thus, it is respectfully submitted that the Examiner's obviousness rejection is in error and based on an incorrect characterization of Sparks. Namely, the Examiner's obviousness rejection presumes that the device of Fig. 4 is a pressure sensor, and that it would be obvious to measure pressure with that device. However, the device of Fig. 4 of Sparks is not a pressure sensor.

For the foregoing reasons, the rejection of claim 27 is in error and should be reversed.

Third Claim Grouping: Claim 28 is not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claims 28

1. Claims 28 Depends From Claim 27

As an initial matter, claim 28 depends from and incorporates all of the limitations of claim 27. Accordingly, claim 28 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 27.

2. Additional Limitations of Claim 28

Claim 28 recites the following additional limitations:

> wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer

3. Sparks Does Not Teach a Protective Layer

In addition to the reasons set forth in connection with claim 27, claim 28 is patentable over Sparks because Sparks fails to teach or suggest a protective layer. With regard to the additional elements of claim 28, the Examiner merely concluded that "Sparks also teaches a protective layer". It is believed that the Examiner contends that the wafer 56 of Sparks constitutes the protective layer. Even if it were assumed that the metal contacts 58b and 58a constituted a "capacitor", which they do not, the wafer 56 is not a *protective layer* because it leaves large portions of the metal contact 58b exposed. In other words, the wafer 56 is merely a support on which the metal contact 58b is placed, it is *not* a protective layer.

As a consequence, Sparks does not teach a "protective layer" as claimed in claim 28. It

is therefore respectfully submitted that claim 28 is allowable over Sparks for reasons independent of those set forth above in connection with claim 27.

Fourth Claim Grouping: Claim 25 is Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 25

1. Claims 25 Depends From Claim 17

As an initial matter, claim 25 depends from and incorporates all of the limitations of claim 17. Accordingly, claim 25 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 17.

2. Additional Limitations of Claim 25

Claim 25 recites the following additional limitations:

> forming said capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first and second metal plates separated by a void

2. The Obviousness Combination is Based on a Mischaracterization of Sparks

The Examiner appears to rely on Sparks for the teaching of the formation of the capacitor using first and second plates. As discussed above in connection with claim 27, Sparks does not teach the formation of a capacitive pressure sensor at all. Thus, there is no motivation or suggestion to form a capacitor using two plates as taught by Sparks and then use that capacitor to measure pressure, as required by claim 25.

Accordingly, for reasons independent of those discussed above in connection with claim 17, it is submitted that claim 25 is allowable over the combination of Smesny, Fisher and Sparks.

For all of the above reasons, the rejection of claim 25 is in error and should be reversed.

Sixth Claim Grouping: Claim 26 is Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 26

1. Claim 26 depends from Claim 25

As an initial matter, claim 26 depends from and incorporates all the limitations of claim 25. Accordingly, claim 26 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 25.

2. Additional Limitations of Claim 26

Claim 26 further includes the following additional limitations:

> wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer

As discussed above in connection with claim 28, Sparks does not disclose a protective layer as claimed. Accordingly, for reasons independent of those discussed above in connection with claim 25, it is respectfully submitted that claim 26 is allowable over the cited art.

(9) CONCLUSION

For all of the foregoing reasons, claims 17, 19, 20 and 25-28 are not unpatentable under 35 U.S.C. § 103, and the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,

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CLAIM APPENDIX

1. (withdrawn) A semiconductor wafer, comprising:

a surface, and

a pressure measurement device supported on said surface of said semiconductor wafer.

2. (withdrawn) The semiconductor wafer of claim 1, wherein:

said pressure measurement device includes a capacitor.

3. (withdrawn) The semiconductor wafer of claim 2, wherein:

said capacitor includes (i) a first metal plate, (ii) a second metal plate, and (iii) a dielectric interposed said first metal plate and said second metal plate.

4. (withdrawn) The semiconductor wafer of claim 2, further comprising:

a protective layer supported on said surface of said semiconductor wafer so that said capacitor is interposed said protective layer and said surface of said semiconductor wafer.

5. (withdrawn) The semiconductor wafer of claim 3, further comprising:

a channel defined in said protective layer such that said channel is in fluid communication with (i) said first metal plate of said capacitor and (ii) an area external to said channel.

6. (withdrawn) The semiconductor wafer of claim 2, further comprising:

capacitance measurement circuitry supported on said surface of said semiconductor wafer, said capacitance measurement circuitry being electrically coupled to said capacitor;

capacitance to pressure conversion circuitry supported on said surface of said semiconductor wafer, said capacitance to pressure conversion circuitry being electrically coupled to said capacitance measurement circuitry; and

pressure data storage circuitry supported on said surface of said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

7. (withdrawn) The semiconductor wafer of claim 6, further comprising:

current time circuitry supported on said surface of said semiconductor wafer, said current time circuitry being electrically coupled to said pressure data storage circuitry.

8. (withdrawn) The semiconductor wafer of claim 6, further comprising:

transmitter circuitry supported on said surface of said semiconductor wafer, said transmitter circuitry being electrically coupled to said pressure data storage circuitry.

9. (withdrawn) An arrangement for measuring pressure, comprising:

a semiconductor wafer;

a capacitor supported on said semiconductor wafer;

capacitance measurement circuitry supported on said semiconductor wafer, said capacitance measurement circuitry being electrically coupled to said capacitor; and

capacitance to pressure conversion circuitry supported on said semiconductor wafer, said capacitance to pressure conversion circuitry being electrically coupled to said capacitance measurement circuitry.

10. (withdrawn) The arrangement of claim 9, wherein:

said capacitor includes a first metal plate and a second metal plate,

said first metal plate being spaced apart from said second metal plate so as to create a void interposed said first metal plate and said second metal plate.

11. (withdrawn) The arrangement of claim 10, wherein:

said void interposed said first metal plate and said second metal plate is a vacuum.

12. (withdrawn) The arrangement of claim 9, further comprising:

a protective layer supported on said semiconductor wafer so that said capacitor is interposed said protective layer and said semiconductor wafer.

13. (withdrawn) The arrangement of claim 12, further comprising:

a channel defined in said protective layer such that said channel is in fluid communication with (i) an exterior surface of said first metal plate of said capacitor and (ii) an area external to said channel.

14. (withdrawn) The arrangement of claim 9, further comprising:

pressure data storage circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

15. (withdrawn) The arrangement claim 14, further comprising:

current time circuitry supported on said semiconductor wafer, said current time circuitry being electrically coupled to said pressure data storage circuitry.

16. (withdrawn) The arrangement of claim 15, further comprising:

transmitter circuitry supported on said semiconductor wafer, said transmitter circuitry being electrically coupled to said pressure data storage circuitry.

17. A method of fabricating a semiconductor wafer, comprising:

(a) subjecting said semiconductor wafer to a pressure; and

(b) measuring said pressure said semiconductor is subjected to with a pressure measurement device supported on said semiconductor wafer, said pressure measurement device including (i) a capacitor, (ii) capacitance measurement circuitry electrically coupled to said capacitor, and (iii) capacitance to pressure conversion circuitry electrically coupled to said capacitance measurement icruity, and further including converting a capacitance of said capacitor to a pressure with said capacitance to pressure conversion circuitry.

19. The method of claim 17, further comprising:

(c) storing said pressure in pressure data storage circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

20. The method of claim 17, further comprising:

(d) transmitting a signal indicative of said pressure to a receiver with transmitter circuitry which is (i) electrically coupled to said capacitance to pressure conversion circuitry and (ii) supported on said semiconductor wafer.

21. The method of claim 19, further comprising:

(d) associating said pressure stored in said pressure data storage circuitry with current time via current time circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said current time circuitry.

22. The method of claim 21, further comprising:

(c) activating said pressure measurement device via a switch supported on said semiconductor wafer.

23. The method of claim 17, further comprising:

(d) deactivating said arrangement via said switch.

24. The method of claim 23, further comprising:

(c) activating said pressure measurement device via a switch supported on said semiconductor wafer.

25. The method of claim 17, further comprising, before step (a), forming said capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first and second metal plates separated by a void.

26. The method of claim 25 wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer.

27. A method of fabricating a semiconductor wafer, comprising:

(a) forming a capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor wafer, the first and second metal plates separated by a void;

(b) subjecting said semiconductor wafer to a pressure; and

(c) measuring said pressure said semiconductor wafer is subjected to using the capacitor.

28. The method of claim 27 wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer.

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(Date of Deposit)

Harold C. Moore
Name of person mailing document or fee

Signature

December 8, 2003
Date of Signature

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	Filed:	September 21, 2001
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	For:	Arrangement for Measuring Pressure on a Semiconductor Wafer and an Associated Method for Fabricating a Semiconductor Wafer
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	Examiner:	Viktor Simkovic
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BRIEF ON APPEAL

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Claim 19 further recites that pressure data storage circuitry is supported on the semiconductor wafer, and that this circuitry is electrically coupled to the capacitance to pressure conversion circuitry. (See, e.g. Fig. 53 and specification at p.11, lines 16-20). Claim 20 further recites transmission of pressure information to a receiver using an on-chip transmitter. (See, e.g. Fig. 53 and specification at p.20, lines 8-14).

In other embodiments, the method of the invention includes first forming the capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first

and second metal plates separated by a void. (See, e.g. plates 32, 34 of Fig. 20 and specification at p.14, lines 12-20). In yet other embodiments, a protecting layer is supported on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer. This provides protection of the metal plate of the capacitor from exposure to certain substances. (See, e.g. specification at p.14, line 21 to p.16, line 2.)

(6) ISSUES

Whether claims 17 and 19-20 are unpatentable under 35 U.S.C. § 103 as obvious over U.S. Patent No. 5,444,637 to Smesny et al. (hereinafter "Smesny") in view of U.S. Patent No. 6,378,378 to Fisher (hereinafter "Fisher");

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Whether 25 and 26 are unpatentable under 35 U.S.C. § 103 as obvious over Smesny in view of Fisher in further view of Sparks.

(7) GROUPING OF CLAIMS

The claims do not all stand or fall together.

Claims 17, 19 and 20 form a first separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 27 forms a second separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 28 forms a third separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 25 forms a fourth separately patentable group which is argued independently of the other claims for purposes of this appeal.

Claim 26 forms a fifth separately patentable group which is argued independently of the other claims for purposes of this appeal.

(8) ARGUMENT

First Claim Grouping: Claims 17, 19 and 20 Are Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 17

1. Claim 17

Claim 17 includes the following limitations:

> measuring said pressure said semiconductor is subjected to with a pressure measurement device supported on said semiconductor wafer, said pressure measurement device including (i) a capacitor, (ii) capacitance measurement circuitry electrically coupled to said capacitor;

2. Smesny Does Not Teach Measuring Pressure with a Capacitor

As admitted by the Examiner, Smesny does not teach or suggest measuring pressure with the pressure measurement device that includes a capacitor and a capacitance measurement circuit electrically coupled to the capacitor. (See e.g. June 25, 2003 Office Action at p.3). Smesny instead suggests that sensors may be implemented to measure pressure conditions on a semiconductor, wherein the pressure sensors may comprise transducers that include resistive circuits. (See Smesny at col. 9, lines 32-44).

3. No Motivation or Suggestion to Modify Smesny With Fisher

Instead, the Examiner relies on Fisher to provide the teaching that a pressures sensor disposed on the semiconductor of Smesny may be a capacitive MEMs pressure sensor. (See June 25, 2003 Office Action at p.3). However, it is respectfully submitted that there is no legally sufficient motivation or suggestion to combine the use of a capacitive MEMs pressure sensor as taught by Fisher in the device of Smesny.

In particular, the Examiner set forth the following reasoning for combining Smesny and Fisher:

> What Smesny et al. fail to specifically teach is the use of a capacitive pressure sensor. This is taught by Fisher in column 3, lines 21-27, where Fisher specifically mentions "capacitive MEMs pressure sensors". . . . Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a capacitive pressure sensor with the method of Smesny et al., since this type of sensor is well suited to be incorporated onto a substrate, as Fisher suggests.

(June 25, 2003 office action at p.3) (emphasis added).

Applicant submits that Fisher does not teach that a capacitive pressure sensor is "well suited" for use in Smesny. Smesny specifically teaches the use of sensors that are *fabricated* in the silicon wafer. Smesny does not suggest or imply that sensors may be separately fabricated and then attached to the semiconductor using adhesives. Yet Fisher only teaches that capacitive MEMs pressures sensors can be separately formed and then attached by adhesives. There is no motivation or suggestion that capacitive MEMs pressure sensors may be "fabricated upon" the wafer of Smesny, nor that it is advantageous to abandon the teachings of Smesny and instead use separately fabricated sensors and attach them to the wafer using an adhesive.

More specifically, Smesny clearly teaches the use of integrally formed sensors, which is much different than separately assembling sensors onto the substrate. Referring to Smesny:

> Sensors 12 described herein are necessary for detecting various processing conditions, and are *fabricated upon* wafer 10 according to well known semiconductor transducer design.

. . .

> Sensors 12 may also be used to measure pressure, force or strain placed at select regions across wafer 10. There are may types of pressure transducers capable of measuring the atmospheric pressure exerted upon the wafer. A suitable pressure transducer includes a diaphragm-type transducer, wherein a diaphragm or elastic element senses pressure and produces a corresponding strain or deflection which can then be read by a bridge circuit connected to the diaphragm or cavity behind the diaphragm. *Another suitable pressure transducer may include a piezoresistive material placed within the semiconductor substrate of wafer 10. The piezoresistive material is formed by diffusing doping compounds into the substrate.* The resulting piezoresistive material produces output current proportional to the amount of pressure or strain exerted thereupon.

(Smesny at col. 8, lines 63-66 and col. 9, lines 28-43) (emphasis added).

Thus, Smesny specifically teaches the use of integrally formed sensors that are fabricated on the substrate. There is no suggestion that separately formed sensors (attached by adhesive) will be suitable or desirable for the circuit of Smesny.

By contrast, Fisher clearly teaches that when capacitive sensors are use, they are used as separately fabricated sensors that are attached using adhesives:

> A number of pressure sensors 12 have been attached to a surface 14 of the wafer with epoxy adhesive 16. The sensors could be attached to the wafer using other adhesives, such as silicone or urethane adhesives. The sensors could be a variety of sensors, such as capacitive MEMS pressure sensors . . . .
>
> . . .
>
> The sensors are packaged pressure sensors, such as the Model 7000-1 sold by ADVANCED CUSTOME SENSORS, INC., the Model EPI-41 sold by ENRAN®, SENSEON™ pressure sensors sold by MOTOROLA, or similar sensors.

(Fisher at col. 3, lines 21-41)

Thus, to the extent Fisher teaches the use of a capacitive sensor, it teaches a *separately-formed* capacitive sensor, which is *not* suitable for use in Smesny. While separately formed sensors may be useful in Fisher, where none of the conversion or data circuitry is located on the chip, such separately formed sensors would be less useful in Smesny, where more circuitry and a greater number of sensors are employed on chip.

To this end, Fisher itself suggests that separately formed sensors are not suitable for use in wafers that incorporate additional conversion and processing circuitry for the pressure measurements. In particular, Fisher discloses one embodiment that does in fact employ integrally formed sensors, although the integrally formed sensors are not *capacitive* pressure sensors. (Fisher at col. 4, line 40 to col. 5, line 26). In any event, Fisher teaches that if integrated (i.e. non-capacitive) sensors, are used, then other circuits may be included on the wafer, including circuits that balance, amplify or buffer the sensor signals. (*Id.* at col. 4, lines 61-65). The clear implication is that the use of *separately* fabricated sensors does *not* lend itself to the inclusion of other supporting circuitry.

Because Fisher only teaches the use of capacitive pressure sensors that are separately fabricated, the resulting teaching of Fisher is that capacitive pressure sensors are not suitable for wafers that include other circuitry that assists in obtaining or processing the measured pressure information. Because Smesny teaches a circuit that employs such other circuitry, including a signal conditioning circuit and a processor, Fisher would only suggest, if anything, the use of integrally-formed, non-capacitive sensors, and not separately fabricated capacitive sensors.

For the above reasons, it is respectfully submitted that the Examiner has failed to make out a prima facie case of obviousness. Specifically, there is no legally sufficient motivation or suggestion in the prior art to employ the capacitive MEMS pressure sensors into the circuit disclosed in Smesny. As a consequence, the rejection of claim 17 should be reversed.

Discussion re: Patentability of Claim 19 and 20

Claims 19 and 20 both depend from and incorporate all of the limitations of claim 17. Accordingly, for at least the same reasons as those set forth above in connection with claim 17, it is respectfully submitted that claims 19 and 20 are patentable over the prior art.

Second Claim Grouping: Claims 27 is not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 27

1. Claim 27

Claim 27 includes the following limitations:

(a) forming a capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor wafer, the first and second metal plates separated by a void;

(b) subjecting said semiconductor wafer to a pressure; and

(c) measuring said pressure said semiconductor wafer is subjected to using the capacitor

2. Sparks Does Not Teach Use of a Capacitor to Measure Pressure

Sparks does not teach or suggest the use of a capacitor to measure pressure, as required by step (c) of claim 27. Nevertheless, in the June 25, 2003 office action, the Examiner provided the following reasoning for the obviousness rejection:

> Sparks teaches a method of forming a semiconductor wafer by fabricating first and second metal plates on the wafer separated by a void (Fig. 4). Sparks does not specifically include the steps of subjecting the wafer to pressure and measuring said pressure using the capacitor, but this is in fact the method of using the pressure sensor taught by Sparks. It would have been obvious to one or ordinary skill in the art at the time of the invention to use the pressure sensor in this way.

(June 25, 2004 office action at pp.3-4)

Applicants disagree that the device illustrated in Fig. 4 of Sparks represents a pressure sensor. The illustrated device indeed has first and second metal plates, but it is not a pressure sensor. The device of Fig. 4 of Sparks is an accelerometer. (Sparks at col. 3, lines 66-67). As a consequence, the Examiner's reasoning that it would have been obvious to "use the pressure sensor in this way" is based on an incorrect premise.

Nevertheless, Sparks does teach a pressure sensor. However, that pressure sensor is piezoresistive, not capacitive. (Sparks at col. 3, lines 53-55). Thus, while it may have been obvious to measure pressure using the *piezoresistive* pressure sensor of Sparks (Fig. 1), there is no teaching to measure pressure using the capacitive accelerometer of Fig. 4. The use of the piezoresistive pressure sensor of Sparks to measure pressure does not arrive at the invention of claim 27.

A pressure sensor and an accelerometer are not the same device. To this end, Sparks clearly distinguishes between pressure sensors and accelerometers, highlighting that those devices are *not* one in the same. (E.g. *id.* at col. 3, lines 53-67 and col. 4, lines 8-17).

Thus, it is respectfully submitted that the Examiner's obviousness rejection is in error and based on an incorrect characterization of Sparks. Namely, the Examiner's obviousness rejection presumes that the device of Fig. 4 is a pressure sensor, and that it would be obvious to measure pressure with that device. However, the device of Fig. 4 of Sparks is not a pressure sensor.

For the foregoing reasons, the rejection of claim 27 is in error and should be reversed.

Third Claim Grouping: Claim 28 is not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claims 28

1. Claims 28 Depends From Claim 27

As an initial matter, claim 28 depends from and incorporates all of the limitations of claim 27. Accordingly, claim 28 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 27.

2. Additional Limitations of Claim 28

Claim 28 recites the following additional limitations:

> wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer

3. Sparks Does Not Teach a Protective Layer

In addition to the reasons set forth in connection with claim 27, claim 28 is patentable over Sparks because Sparks fails to teach or suggest a protective layer. With regard to the additional elements of claim 28, the Examiner merely concluded that "Sparks also teaches a protective layer". It is believed that the Examiner contends that the wafer 56 of Sparks constitutes the protective layer. Even if it were assumed that the metal contacts 58b and 58a constituted a "capacitor", which they do not, the wafer 56 is not a *protective layer* because it leaves large portions of the metal contact 58b exposed. In other words, the wafer 56 is merely a support on which the metal contact 58b is placed, it is *not* a protective layer.

As a consequence, Sparks does not teach a "protective layer" as claimed in claim 28. It

is therefore respectfully submitted that claim 28 is allowable over Sparks for reasons independent of those set forth above in connection with claim 27.

Fourth Claim Grouping: Claim 25 is Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 25

1. Claims 25 Depends From Claim 17

As an initial matter, claim 25 depends from and incorporates all of the limitations of claim 17. Accordingly, claim 25 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 17.

2. Additional Limitations of Claim 25

Claim 25 recites the following additional limitations:

> forming said capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first and second metal plates separated by a void

2. The Obviousness Combination is Based on a Mischaracterization of Sparks

The Examiner appears to rely on Sparks for the teaching of the formation of the capacitor using first and second plates. As discussed above in connection with claim 27, Sparks does not teach the formation of a capacitive pressure sensor at all. Thus, there is no motivation or suggestion to form a capacitor using two plates as taught by Sparks and then use that capacitor to measure pressure, as required by claim 25.

Accordingly, for reasons independent of those discussed above in connection with claim 17, it is submitted that claim 25 is allowable over the combination of Smesny, Fisher and Sparks.

For all of the above reasons, the rejection of claim 25 is in error and should be reversed.

Sixth Claim Grouping: Claim 26 is Not Obvious Over the Cited Prior Art

Discussion re: Patentability of Claim 26

1. <u>Claim 26 depends from Claim 25</u>

As an initial matter, claim 26 depends from and incorporates all the limitations of claim 25. Accordingly, claim 26 is patentable over the prior art for at least the same reasons as those set forth above in connection with claim 25.

2. <u>Additional Limitations of Claim 26</u>

Claim 26 further includes the following additional limitations:

> wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer

As discussed above in connection with claim 28, Sparks does not disclose a protective layer as claimed. Accordingly, for reasons independent of those discussed above in connection with claim 25, it is respectfully submitted that claim 26 is allowable over the cited art.

(9) CONCLUSION

For all of the foregoing reasons, claims 17, 19, 20 and 25-28 are not unpatentable under 35 U.S.C. § 103, and the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,

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CLAIM APPENDIX

1. (withdrawn) A semiconductor wafer, comprising:

a surface, and

a pressure measurement device supported on said surface of said semiconductor wafer.

2. (withdrawn) The semiconductor wafer of claim 1, wherein:

said pressure measurement device includes a capacitor.

3. (withdrawn) The semiconductor wafer of claim 2, wherein:

said capacitor includes (i) a first metal plate, (ii) a second metal plate, and (iii) a dielectric interposed said first metal plate and said second metal plate.

4. (withdrawn) The semiconductor wafer of claim 2, further comprising:

a protective layer supported on said surface of said semiconductor wafer so that said capacitor is interposed said protective layer and said surface of said semiconductor wafer.

5. (withdrawn) The semiconductor wafer of claim 3, further comprising:

a channel defined in said protective layer such that said channel is in fluid communication with (i) said first metal plate of said capacitor and (ii) an area external to said channel.

6. (withdrawn) The semiconductor wafer of claim 2, further comprising:

capacitance measurement circuitry supported on said surface of said semiconductor wafer, said capacitance measurement circuitry being electrically coupled to said capacitor;

capacitance to pressure conversion circuitry supported on said surface of said semiconductor wafer, said capacitance to pressure conversion circuitry being electrically coupled to said capacitance measurement circuitry; and

pressure data storage circuitry supported on said surface of said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

7. (withdrawn) The semiconductor wafer of claim 6, further comprising:

current time circuitry supported on said surface of said semiconductor wafer, said current time circuitry being electrically coupled to said pressure data storage circuitry.

8. (withdrawn) The semiconductor wafer of claim 6, further comprising:

transmitter circuitry supported on said surface of said semiconductor wafer, said transmitter circuitry being electrically coupled to said pressure data storage circuitry.

9. (withdrawn) An arrangement for measuring pressure, comprising:

a semiconductor wafer;

a capacitor supported on said semiconductor wafer;

capacitance measurement circuitry supported on said semiconductor wafer, said capacitance measurement circuitry being electrically coupled to said capacitor; and

capacitance to pressure conversion circuitry supported on said semiconductor wafer, said capacitance to pressure conversion circuitry being electrically coupled to said capacitance measurement circuitry.

10. (withdrawn) The arrangement of claim 9, wherein:

said capacitor includes a first metal plate and a second metal plate,

said first metal plate being spaced apart from said second metal plate so as to create a void interposed said first metal plate and said second metal plate.

11. (withdrawn) The arrangement of claim 10, wherein:

said void interposed said first metal plate and said second metal plate is a vacuum.

12. (withdrawn) The arrangement of claim 9, further comprising:

a protective layer supported on said semiconductor wafer so that said capacitor is interposed said protective layer and said semiconductor wafer.

13. (withdrawn) The arrangement of claim 12, further comprising:

a channel defined in said protective layer such that said channel is in fluid communication with (i) an exterior surface of said first metal plate of said capacitor and (ii) an area external to said channel.

14. (withdrawn) The arrangement of claim 9, further comprising:

pressure data storage circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

15. (withdrawn) The arrangement claim 14, further comprising:

current time circuitry supported on said semiconductor wafer, said current time circuitry being electrically coupled to said pressure data storage circuitry.

16. (withdrawn) The arrangement of claim 15, further comprising:

transmitter circuitry supported on said semiconductor wafer, said transmitter circuitry being electrically coupled to said pressure data storage circuitry.

17. A method of fabricating a semiconductor wafer, comprising:

(a) subjecting said semiconductor wafer to a pressure; and

(b) measuring said pressure said semiconductor is subjected to with a pressure measurement device supported on said semiconductor wafer, said pressure measurement device including (i) a capacitor, (ii) capacitance measurement circuitry electrically coupled to said capacitor, and (iii) capacitance to pressure conversion circuitry electrically coupled to said capacitance measurement icruity, and further including converting a capacitance of said capacitor to a pressure with said capacitance to pressure conversion circuitry.

19. The method of claim 17, further comprising:

(c) storing said pressure in pressure data storage circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said capacitance to pressure conversion circuitry.

20. The method of claim 17, further comprising:

(d) transmitting a signal indicative of said pressure to a receiver with transmitter circuitry which is (i) electrically coupled to said capacitance to pressure conversion circuitry and (ii) supported on said semiconductor wafer.

21. The method of claim 19, further comprising:

(d) associating said pressure stored in said pressure data storage circuitry with current time via current time circuitry supported on said semiconductor wafer, said pressure data storage circuitry being electrically coupled to said current time circuitry.

22. The method of claim 21, further comprising:

(c) activating said pressure measurement device via a switch supported on said semiconductor wafer.

23. The method of claim 17, further comprising:

(d) deactivating said arrangement via said switch.

24. The method of claim 23, further comprising:

(c) activating said pressure measurement device via a switch supported on said semiconductor wafer.

25. The method of claim 17, further comprising, before step (a), forming said capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor, the first and second metal plates separated by a void.

26. The method of claim 25 wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer.

27. A method of fabricating a semiconductor wafer, comprising:

(a) forming a capacitor on the semiconductor by fabricating first and second metal plates on the semiconductor wafer, the first and second metal plates separated by a void;

(b) subjecting said semiconductor wafer to a pressure; and

(c) measuring said pressure said semiconductor wafer is subjected to using the capacitor.

28. The method of claim 27 wherein forming the capacitor on the semiconductor further comprises supporting a protecting layer on the semiconductor wafer so that the capacitor is interposed between said protective layer and said semiconductor wafer.